

WHAT IS CLAIMED IS:

- 1 1. A multi-layer semiconductor wafer structure defining a multiplicity of dies formed
2 thereon, said wafer structure comprising:
3 a first scribe line having a selected width extending along a first direction and adjacent a
4 first die of said multiplicity of dies;
5 a second scribe line having a selected width extending along a second direction adjacent
6 said first die and intersecting said first scribe line at a corner point of said first die;
7 at least one free area defined on at least one of said first and second scribe lines where
8 placement of a test key is restricted.
- 1 2. The multi-layer semiconductor wafer structure of claim 1 wherein at least one layer of
2 said wafer structure is a low-k dielectric layer.
- 1 3. The multi-layer semiconductor wafer structure of claim 1 wherein the low-k dielectric
2 layer has a dielectric constant of less than approximately 3.5.
- 1 4. The multi-layer semiconductor wafer structure of claim 3 wherein the low-k dielectric
2 layer has a dielectric constant of less than 3.0.
- 1 5. The multi-layer semiconductor wafer structure of claim 1 wherein the low-k dielectric
2 layer is a material selected from the group consisting of CVD, SiOC, SiOCN, Spin-on SiOC,
3 CVD polymer, Spin-on polymer, FSG, SiO₂ and combinations thereof.
- 1 6. The multi-layer semiconductor wafer structure of claim 1 wherein said free area is a free
2 area A₁ on the first scribe line and is defined by the equation $A_1 = D_1 \times S_1$ where D₁ is the distance

3 along the first direction extending from the corner point of the die, and S_1 is the width of the first
4 scribe line.

1 7. The multi-layer semiconductor wafer structure of claim 1 wherein the free area is defined
2 on the top of the multi-layer structure.

1 8. The multi-layer semiconductor wafer structure of claim 1 wherein the free area is defined
2 on at least one of the top three layers of the multi-layer structure.

1 9. The multi-layer semiconductor wafer structure of claim 6 further comprising at least one
2 test key formed in said free area, said at least one test key having a measurement ratio R_1 ,
3 wherein the measurement ratio is defined by the equation: $R_1 = M_1/A_1$, wherein M_1 is the total
4 area of said at least one test key formed on the free area A_1 , and R_1 is less than about 10%.

1 10. The multi-layer semiconductor wafer structure of claim 6 wherein the distance D_1 is less
2 than about $600\mu\text{m}$.

1 11. The multi-layer semiconductor wafer structure of claim 6 wherein the width S_1 of the first
2 scribe line is greater than about $20\mu\text{m}$.

1 12. The multi-layer semiconductor wafer structure of claim 1 wherein the multi-layer
2 structure is formed on a substrate selected from the group consisting of bulk Si, SOI, SiGe,
3 GaAs, InP, and a combination thereof.

1 13. The multi-layer semiconductor wafer structure of claim 1 wherein said first die
2 comprises:

3 a first peripheral region inside of and extending parallel to said first scribe line;
4 a second peripheral region inside of and extending parallel to said second scribe line and
5 intersecting said first peripheral region to form a corner area;
6 a conductive ring formed between said die and said first peripheral region and said
7 second peripheral region; and
8 an array of apertures formed in the conductive ring and adjacent the corner area of the
9 die.

1 14. The multi-layer semiconductor wafer structure of claim 13 wherein said array of
2 apertures comprises at least two slots.

1 15. The multi-layer semiconductor wafer structure of claim 13 wherein said array of
2 apertures comprises two rows of holes.

1 16. The multi-layer semiconductor wafer structure of claim 13 wherein the array of apertures
2 extends along at least one of the first peripheral region and the second peripheral region.

1 17. The multi-layer semiconductor wafer structure of claim 13 wherein the die further
2 comprises a circuit area with a plurality of circuit elements, wherein the conductive ring is
3 electrically connected to the circuit elements to apply one of a power source and a ground
4 potential to the circuit elements.

1 18. The multi-layer semiconductor wafer structure of claim 13 wherein the conductive ring
2 has a width of between 50 μ m and about 300 μ m.

1 19. The multi-layer semiconductor wafer structure of claim 1 wherein said free area is a free
2 area A_S at the intersection of said first scribe line and said second scribe line and is defined by
3 the equation $A_S=S_1 \times S_2$, wherein S_1 is the width of the first scribe line and S_2 is the width of the
4 second scribe line.

1 20. The multi-layer semiconductor wafer structure of claim 19 further comprising at least one
2 test key formed on said free area A_S , said test key having a measurement ratio R_S that is less than
3 10% and is defined by the equation $R_S=M_S/A_S$, wherein M_S is the total area of said at least one
4 test key formed on the free area A_S .

1 21. The multi-layer semiconductor wafer structure of claim 19 wherein the width of the
2 scribe lines S_1 and S_2 is greater than about $20\mu\text{m}$.

1 22. The multi-layer semiconductor wafer structure of claim 1 wherein said at least one free
2 area comprises a first free area A_1 on the first scribe line and a second free area A_2 on the second
3 scribe line, said first free area defined by the equation $A_1=D_1 \times S_1$ where D_1 is the distance along
4 the first direction extending from the corner point of the die and S_1 is the width of the first scribe
5 line, said second free area defined by the equation $A_2=D_2 \times S_2$ where D_2 is the distance along the
6 second direction extending from the corner point of the die and S_2 is the width of the second
7 scribe line.

1 23. The multi-layer semiconductor wafer structure of claim 22 comprising a third free area
2 A_S at the intersection of said first scribe line and said second scribe line and is defined by the
3 equation $A_S=S_1 \times S_2$.

1 24. The multi-layer semiconductor wafer structure of claim 23 further comprising:
2 at least one test key formed on at least one of the free areas A_1 , A_2 and A_S ;
3 wherein a first measurement ratio R_1 is defined as the equation $R_1=M_1/A_1$, wherein M_1 is
4 the total area of the test keys formed on the first free area A_1 ;
5 wherein a second measurement ratio R_2 is defined as the equation $R_2=M_2/A_2$, wherein M_2
6 is the total area of the test keys formed on the second free area A_2 ;
7 wherein a third measurement ratio R_S is defined as the equation $R_S=M_S/A_S$, wherein M_S
8 is the total area of the test keys formed on the third area A_S ; and
9 wherein a total measurement ratio R is defined as the equation $R=(M_1+M_2+M_S) /$
10 $(A_1+A_2+A_S)$.

1 25. The multi-layer semiconductor wafer structure of claim 24 wherein R_1 is less than about
2 10%.

1 26. The multi-layer semiconductor wafer structure of claim 24 wherein R_2 is less than about
2 10%.

1 27. The multi-layer semiconductor wafer structure of claim 24 wherein R_S is less than about
2 10%.

1 28. The multi-layer semiconductor wafer structure of claim 24 wherein the ratio R is less
2 than about 10%.

1 29. The multi-layer semiconductor wafer structure of claim 24 wherein the first distance D_1
2 is less than about 600 μm .

1 30. The multi-layer semiconductor wafer structure of claim 24 wherein the second distance
2 D_2 is less than about $600\mu\text{m}$.

1 31. The multi-layer semiconductor wafer structure of claim 24 wherein the width S_1 of the
2 first scribe line is greater than about $20\mu\text{m}$.

1 32. The multi-layer semiconductor wafer structure of claim 24 wherein the width S_2 of the
2 second scribe line is greater than about $20\mu\text{m}$.

1 33. A multi-layer semiconductor wafer structure defining a multiplicity of dies formed
2 thereon, said wafer structure comprising:

3 a first scribe line having a selected width extending along a first direction;

4 a second scribe line having a selected width extending along a second direction and
5 intersecting said first scribe line;

6 four dies located at and separated by the intersection of said first and second scribe lines
7 wherein each of the four dies comprises a corner point adjacent the intersection of said first and
8 second scribe lines;

9 a first free area A_1 on the first scribe line adjacent the corner point of the first die,
10 wherein A_1 is defined by the equation $A_1 = D_1 \times S_1$ and wherein D_1 is the distance extending from
11 the corner point of the first die, and S_1 is the width of the first scribe line;

12 a second free area A_2 on the second scribe line adjacent the corner point of the second
13 die, wherein A_2 is defined by the equation $A_2 = D_2 \times S_2$, and wherein D_2 is the distance from the
14 corner point of the second die, and S_2 is the width of the second scribe line;

15 a third free area A_3 on the second scribe line adjacent the third corner point of the third
16 die, wherein A_3 is defined by the equation $A_3 = D_3 \times S_2$, and wherein D_3 is the distance from the

17 corner point of the third die;
18 a fourth free area A_4 on the first scribe line adjacent the corner point of the fourth die,
19 wherein A_4 is defined by the equation $A_4=D_4 \times S_1$, and wherein D_4 is the distance from the corner
20 point of the fourth die; and
21 a fifth free area A_5 on the intersection of the first scribe line and the second scribe line
22 and is defined by the equation $A_5=S_1 \times S_2$.

1 34. The semiconductor wafer of claim 33 further comprising:
2 at least one test key formed on at least one of the free areas A_1 , A_2 , A_3 , A_4 and A_5 ;
3 wherein a first measurement ratio R_1 is defined as the equation $R_1=M_1/A_1$, wherein M_1 is
4 the total area of the test keys formed on the first free area A_1 ;
5 wherein a second measurement ratio R_2 is defined as the equation: $R_2= M_2/A_2$, wherein
6 M_2 is the total area of the test keys formed on the second free area A_2 ;
7 wherein a third measurement ratio R_3 is defined as the equation: $R_3= M_3/A_3$, wherein M_3
8 is the total area of the test keys formed on the third free area A_3 ;
9 wherein a fourth measurement ratio R_4 is defined as the equation: $R_4= M_4/A_4$, wherein
10 M_4 is the total area of the test keys formed on the fourth free area A_4 ;
11 wherein a fifth measurement ratio R_5 is defined as the equation: $R_5= M_5/A_5$, wherein M_5
12 is the total area of the test keys formed on the fifth free area A_5 ; and
13 wherein a total measurement ration R is defined as the equation $R=(M_1+M_2+M_3+M_4+M_5)$
14 $/ (A_1+A_2+A_3+A_4+A_5)$.

1 35. The semiconductor wafer of claim 34 wherein the first measurement ratio R_1 is less than
2 about 10%.

- 1 36. The semiconductor wafer of claim 33 wherein the distance D_4 is less than about $600\mu\text{m}$.
- 1 37. The semiconductor wafer of claim 33 wherein the width S_1 of the first scribe line is
2 greater than about $20\mu\text{m}$.
- 1 38. The semiconductor wafer of claim 33 wherein the width S_2 of the second scribe line is
2 greater than about $20\mu\text{m}$.
- 1 39. The semiconductor wafer of claim 33 wherein the multi-layer structure is formed on a
2 substrate selected from the group consisting of bulk Si, SOI, SiGe, GaAs and InP.
- 1 40. The semiconductor wafer of claim 33 wherein each of said four dies comprises:
2 a first peripheral region parallel to said first scribe line;
3 a second peripheral region parallel to said second scribe line;
4 a conductive ring formed between said die and said first peripheral region and said
5 second peripheral region; and
6 an array of apertures formed in the conductive ring and adjacent the corner area of the
7 die.
- 1 41. The semiconductor wafer of claim 33 wherein the low-k dielectric layer has a dielectric
2 constant less than approximately 3.5.
- 1 42. The semiconductor wafer of claim 40 wherein the array of apertures comprises two rows
2 of holes.

1 43. The semiconductor wafer of claim 41 wherein said array of apertures comprises at least
2 two slots.

1 44. The semiconductor wafer of claim 40 wherein the array of apertures extends along at
2 least one of the first peripheral region and the second peripheral region.

1 45. The semiconductor wafer of claim 40, wherein each of the four dies further comprises a
2 circuit area with a plurality of circuit elements, wherein the conductive ring is electrically
3 connected to the circuit elements to apply one of a power source and a ground potential to the
4 circuit elements.

1 46. The semiconductor wafer of claim 40 wherein the conductive ring has a width of between
2 about 50 μ m and 300 μ m.

1 47. A fabrication method for a multi-layer semiconductor wafer defining a multiplicity of
2 dies, the fabrication method comprising the steps of:

3 providing a semiconductor wafer having a first and second scribe line, wherein a corner
4 point of a die is defined by an intersection of the first scribe line and the second scribe line;

5 defining a free area where the placement of test keys is restricted, the free area being
6 located on the first scribe line adjacent the corner point of the die; and

7 cutting through the first scribe line and the second scribe line to separate the die.

1 48. The method of claim 47 wherein said step of cutting is a method selected from the group
2 consisting of diamond sawing, laser cutting, liquid jet scribing, water jet cutting and
3 combinations of said cutting methods.

1 49. The method of claim 47 wherein the low-k dielectric layer has a dielectric constant less
2 than approximately 3.5.

1 50. The method of claim 47 wherein the low-k dielectric layer is selected from the group
2 consisting of CVD, SiOC, SiOCN, Spin-on SiOC, CVD polymer, Spin-on polymer, FSG and
3 SiO₂.

1 51. The method of claim 47 wherein said free area is the free area A₁ on the first scribe line
2 and is defined by the equation $A_1 = D_1 \times S_1$, where D₁ is the distance along the first direction
3 extending from the corner point of the die and S₁ is the width of the first scribe line.

1 52. The method of claim 51 further comprising the step of forming at least one test key on
2 the free area A₁ prior to said cutting step and wherein a measurement ratio R₁ is defined by the
3 equation $R_1 = M_1 / A_1$, wherein M₁ is the total area of said at least one test key formed on the free
4 area A₁, and wherein R₁ is less than about 10%.

1 53. The method of claim 51 wherein the distance D₁ is less than about 600μm.

1 54. The method of claim 51 wherein the width S₁ of the first scribe line is greater than about
2 20μm.

1 55. The method of claim 47 comprising the step of forming the multi-layer structure on a
2 substrate selected from a group of materials consisting of bulk Si, SOI, SiGe, GaAs and InP.

1 56. The method of claim 47 further comprising the steps of:
2 defining a first peripheral region inside of and extending parallel to said first scribe line;

3 defining a second peripheral region inside of and extending parallel to said second scribe
4 line;
5 forming a conductive ring between said die and said first peripheral region and said
6 second peripheral region; and
7 forming an array of apertures in the conductive ring and adjacent the corner point of the
8 die.

1 57. The method of claim 56 wherein the step of forming an array of apertures comprises the
2 step of forming at least two slots.

1 58. The method of claim 56 wherein the step of forming an array of apertures comprises the
2 step of forming at least two rows of holes.

1 59. The method of claim 56 further comprising the steps of connecting said conductive ring
2 to circuit elements in said die and connecting a terminal of a source of power to said conductive
3 ring.

1 60. The method of claim 59 further comprising the step of forming at least one test key on
2 the free area A_S prior to said cutting step and wherein a measurement ratio R_S is defined by the
3 equation $R_S = M_S / A_S$, wherein M_S is the total area of said at least one test key formed on the free
4 area A_S , and wherein R_1 is less than about 10%.

1 61. The method of claim 59 wherein the width S_1 of the first scribe line is greater than about
2 $20\mu\text{m}$.

1 62. The method of claim 59 wherein the width S_2 of the second scribe line is greater than
2 about $20\mu\text{m}$.

1 63. The method of claim 47 wherein said free area is the free area A_S at the intersection of
2 the first scribe line and the second scribe line and is defined by the equation $A_S=S_1 \times S_2$, where S_1
3 is the width of the first scribe line and S_2 is the width of the second scribe line.

1 64. The method of claim 63 wherein said step of forming a free area further comprises
2 forming the free area A_1 on the first scribe line and the free area A_2 on the second scribe line,
3 said free area A_1 defined by the equation $A_1=D_1 \times S_1$, where D_1 is the distance along the first
4 direction extending from the corner point of the die and said free area A_2 defined by the equation
5 $A_2=D_2 \times S_2$ where D_2 is the distance along the second direction extending from the corner point of
6 the die.